ABSTRAK

PT TDK ELECTRONICS INDONESIA adalah perusahaan manufaktur komponen elektronik yang menghadapi masalah ketidakseimbangan waktu proses di lini soldering. Proses chip insertion memakan waktu 156 detik per batch, sedangkan press wire dan soldering masing-masing 16,8 dan 32,4 detik. Penelitian ini bertujuan mengusulkan strategi penyeimbangan lintasan menggunakan perencanaan agregat untuk mengurangi *bottleneck,* meminimalkan waktu menganggur, dan meningkatkan efisiensi produksi.

Penelitian ini mencakup perhitungan tiga indikator line balancing: efisiensi lini, penundaan keseimbangan, dan indeks kelancaran. Selain itu, membandingkan hasil produksi aktual dengan target harian, menyesuaikan jumlah stasiun kerja dan operator, serta merencanakan produksi agregat menggunakan tiga metode. Hasilnya dirangkum berdasarkan biaya, tenaga kerja, dan kelebihan serta kekurangan masing-masing metode untuk memilih strategi perbaikan yang paling efisien.

Berdasarkan analisis usulan strategi perencanaan agregat di PT TDK Electronics Indonesia, ditemukan bahwa nilai line efficiency, balance delay, dan smoothness index masing-masing adalah 84%, 16%, dan 5580,1806. Penyesuaian stasiun kerja dan tenaga kerja diperlukan untuk mencapai target output. Tiga strategi perencanaan agregat dianalisis, dan level strategy terpilih sebagai yang terbaik karena biaya terendah dan stabilitas operasional yang tinggi.Berdasarkan penelitian ini, disarankan agar PT TDK ELECTRONICS INDONESIA menerapkan *level strategy* dalam perencanaan agregat, karena metode ini terbukti menghasilkan biaya produksi terendah. Selain itu, penelitian selanjutnya dapat memperluas cakupan dengan menerapkan perencanaan multi-tahun, sehingga hasil perbaikan strategi perencanaan produksi agregat menjadi lebih stabil dan efektif.

Kata kunci: keseimbangan lintasan, perencanaan agregat, efisiensi produksi, *level strategy*

ABSTRACT

PT TDK ELECTRONICS INDONESIA is an electronic component manufacturing company facing the problem of process time imbalance in the soldering line. The chip insertion process takes 156 seconds per batch, while wire pressing and soldering take 16.8 and 32.4 seconds, respectively. This study aims to propose a line balancing strategy using aggregate planning to reduce bottlenecks, minimize idle time, and improve production efficiency.

The study includes calculations of three line balancing indicators: line efficiency, balancing delay, and smoothness index. Additionally, it compares actual production results with daily targets, adjusts the number of workstations and operators, and plans aggregate production using three methods. The results are summarized based on costs, labor, and the advantages and disadvantages of each method to select the most efficient improvement strategy.

Based on the analysis of the proposed aggregate planning strategy at PT TDK Electronics Indonesia, it was found that the values for line efficiency, balance delay, and smoothness index were 84%, 16%, and 5580.1806, respectively. Adjustments to workstations and labor are necessary to achieve the output target. Three aggregate planning strategies were analyzed, and the level strategy was selected as the best due to its lowest cost and high operational stability. Based on this research, it is recommended that PT TDK ELECTRONICS INDONESIA implement the level strategy in aggregate planning, as this method has proven to result in the lowest production costs. Additionally, further research could expand the scope by applying multi-year planning, thereby making the improvements in aggregate production planning strategy more stable and effective.

Keywords: line balancing, aggregate planning, product efficiency, level strategy